CLAIMS:

1. A multi-output DC-DC converter comprising:

an inductor (L),

a main switch (S0) for periodically coupling a DC-input voltage (Vin) to the inductor (L),

a multitude of output switches (S1, S2, S3) coupled to the inductor (L), each one for generating an associated one of a multitude of output voltages (V1, V2, V3) to an associated one of a multitude of loads (L1, L2 , L3), and

a controller (1) for controlling the main switch (S0) and the output switches (S1, S2, S3) in a sequence (SE) of cycles (CY1, CY2, CY3), each one of the cycles (CY1, CY2, CY3) comprising an on-phase (TO1, TO2, TO3) of the main switch (S0) followed by an on-phase (T1, T2, T3) of one of the multitude of the output switches (S1, S2, S3),

the controller (1) comprising:

a multitude of comparators (10, 11, 12) each one for comparing an associated one of the multitude of output voltages (V1, V2, V3) with an associated one of a multitude of reference voltages (VR1, VR2, VR3),

means for determining (13) whether a number of the output voltages (V1, V2, V3) which have a value above their associated reference voltage (VR1, VR2, VR3) is larger than, smaller than, or equal to a number of the multitude of output voltages (V1, V2, V3) which have a value below their associated reference voltage (VR1, VR2, VR3),

means for generating (14) the cycles (CY1, CY2, CY3) either with a first duty cycle (D1) or a second duty cycle (D2) being larger than the first duty cycle (D1) to obtain a first number (N1) of cycles (CY1, CY2, CY3) with the first duty cycle (D1) and a second number (N2) of cycles (CY1, CY2, CY3) with the second duty cycle (D2), the first number (N1) being larger than, smaller than, or equal to the second number (N2), respectively.

2. A multi-output DC-DC converter as claimed in claim 1, wherein the first number (N1) is equal to the number of output voltages (V1, V2, V3) which have a value above their associated reference voltage (VR1, VR2, VR3), and wherein the second number

(N2) is equal to the number of output voltages (V1, V2, V3) which have a value below their associated reference voltage (VR1, VR2, VR3).

3. A multi-output DC-DC converter as claimed in claim 2, wherein the means for generating (14) the cycles comprises a sequencer (140) for controlling an order of the cycles (CY1, CY2, CY3) in a sequence (SE) wherein, as much as possible at the present values of the first number (N1) and the second number (N2), one of the cycles (CY1, CY2, CY3) with the second duty cycle (D2) precedes one of the cycles (CY1, CY2, CY3) with the first duty cycle (D1).

4. A multi-output DC-DC converter as claimed in claim 2, wherein the means for generating (14) the cycles comprises a sequencer (140) for controlling an order of the cycles (CY1, CY2, CY3) in a sequence (SE) to first comprise all the cycles (CY1, CY2, CY3) with the second duty cycle (D2) and then all the cycles (CY1, CY2, CY3) with the first duty cycle (D1).

5. A multi-output DC-DC converter as claimed in claim 2, wherein the means for generating (14) the cycles comprises a means for allocating (141):

the first number (N1) of the first duty cycles (D1) as much as possible to cycles (CY1, CY2, CY3) associated with output voltages (V1, V2, V3) that have a value below their corresponding reference voltage (VR1, VR2, VR3), and

the second number (N2) of the second duty cycles (D2) as much as possible to cycles (CY1, CY2, CY3) associated with output voltages (V1, V2, V3) which have a value above their corresponding reference voltage (VR1, VR2, VR3).

6. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) the number of duty cycles is adapted for further allocating the first duty cycle (D1) to cycles (CY1, CY2, CY3) associated with output voltages (V1, V2, V3) that have a value above their corresponding reference voltage (VR1, VR2, VR3) if the first number (N1) is larger than the number of output voltages (V1, V2, V3) that have a value below their associated reference voltage (VR1, VR2, VR3).

7. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted for further allocating the second duty cycle (D2) to cycles (CY1,

CY2, CY3) associated with output voltages (V1, V2, V3) that have a value below their associated reference voltage (VR1, VR2, VR3) if the second number (N2) is larger than the number of output voltages (V1, V2, V3) that have a value above their associated reference voltage (VR1, VR2, VR3).

8. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted for allocating to a predetermined one of the cycles (CY1, CY2, CY3) in a sequence (SE) wherein a lowest amount of energy is transferred to one of the output voltages (V1, V2, V3) of which the value is above the associated reference voltage (VR1, VR2, VR3).

9. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted for allocating as a first one of the cycle (CY1, CY2, CY3) in a sequence (SE) an output voltage (V1, V2, V3) of which the value is above the associated reference voltage (VR1, VR2, VR3) and to which a first duty cycle (D1) is allocated.

10. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted for allocating to a predetermined one of the cycles (CY1, CY2, CY3) in a sequence (SE) wherein a highest amount of energy is transferred to one of the output voltages (V1, V2, V3) of which the value is below the associated reference voltage (VR1, VR2, VR3).

11. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted for allocating, in a sequence (SE), a last cycle (CY1) to which a second duty cycle is allocated to an output voltage (V1, V2, V3) of which the value is below the associated reference voltage (VR1, VR2, VR3) and to which a second duty cycle (D2) is allocated.

12. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted to allocate in a next sequence (SE) the second duty cycle (D2) to a particular one of the output voltages (V1, V2, V3), if in a preceding sequence (SE) the first duty cycle (D1) is allocated to this particular one of the output voltages (V1, V2, V3) while the associated reference voltage (VR1, VR2, VR3) is lower.

13. A multi-output DC-DC converter as claimed in claim 5, wherein the means for allocating (141) is adapted to allocate in a next sequence (SE) the first duty cycle (D1) to a particular one of the output voltages (V1, V2, V3), if in a preceding sequence (SE) the second duty cycle (D2) is allocated to this particular one of the output voltages (V1, V2, V3) while the associated reference voltage (VR1, VR2, VR3) is higher.

14. A multi-output DC-DC converter as claimed in 1, the multi-output DC-DC converter further comprising mode detectors (15), each one being associated with one of the multiple output voltages (V1, V2, V3) for keeping track of a mode of each one of a multiple outputs (O1, O2, O3), each mode detector having three states (0, 1, 2), a first state (0) indicating whether no load current is drawn from the associated output (O1, O2, O3), a second state (1) and a third state (2) wherein load current is drawn from the associated output (O1, O2, O3), if the associated output (O1, O2, O3) is in the first state (0) and the associated output voltage (V1, V2, V3) is smaller than its associated reference voltage (VR1, VR2, VR3) the third state (2) is entered, if the associated output (O1, O2, O3) is in the first state (0) and the associated output voltage (V1, V2, V3) is larger than its associated reference voltage (VR1, VR2, VR3) the first state (0) will be maintained, if the associated output (O1, O2, O3) is in the second state (1) and the associated output voltage (V1, V2, V3) is larger than its associated reference voltage (VR1, VR2, VR3) the first state (0) is entered, if the associated output (O1, O2, O3) is in the second state (1) and the associated output voltage (V1, V2, V3) is smaller than its associated reference voltage (VR1, VR2, VR3) the third state (2) is entered, if the associated output (O1, O2, O3) is in the third state (2) and the associated output voltage (V1, V2, V3) is smaller than its associated reference voltage (VR1, VR2, VR3) the third state (2) is maintained, if the associated output (O1, O2, O3) is in the third (2) state and the associated output voltage (V1, V2, V3) is larger than its associated reference voltage (VR1, VR2, VR3) the second state (1) is entered.

15. A multi-output DC-DC converter as claimed in 14, the means (14) for generating the cycles further comprising a sequence controller (142) for controlling a number of cycles (CY) required in a sequence (SE) such that cycles (CY) are generated only for outputs (O1, O2, O3) that are in the second state (1) or the third state (2).

16. An apparatus comprising the multi-output DC-DC converter as claimed in claim 1.

17. A method of controlling a multi-output DC-DC converter comprising:

an inductor (L),

a main switch (S0) for periodically coupling a DC-input voltage (Vin) to the inductor (L),

a multitude of output switches (S1, S2, S3) coupled to the inductor (L), each one for supplying an associated one of a multitude of output voltages (V1, V2, V3) to an associated one of a multitude of loads (L1, L2 , L3), the method comprising:

controlling (1) the main switch (S0) and the output switches (S1, S2, S3) in a sequence (SE) of cycles (CY1, CY2, CY3), each one of the cycles (CY1, CY2, CY3) containing an on-phase (TO1, TO2, TO3) of the main switch (S0) followed by an on-phase (T1, T2, T3) of one of the multitude of the output switches (S1, S2, S3),

the controlling (1) comprising:

comparing (10, 11, 12) a corresponding one of the multitude of output voltages (V1, V2, V3) with an associated one of a multitude of reference voltages (VR1, VR2, VR3),

determining (13) whether a number of the output voltages (V1, V2, V3) that have a value above their associated reference voltage (VR1, VR2, VR3), is larger than, smaller than, or equal to a number of the multitude of output voltages (V1, V2, V3) that have a value below their associated reference voltage (VR1, VR2, VR3),

means for generating (14) the cycles (CY1, CY2, CY3) either only with a first duty cycle (D1) or a second duty cycle (D2) being larger than the first duty cycle (D1) to obtain a first number (N1) of cycles (CY1, CY2, CY3) with the first duty cycle (D1) and a second number (N2) of cycles (CY1, CY2, CY3) with the second duty cycle (D2), the first number (N1) being larger than, smaller than, or equal to the second number (N2), respectively.